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EXAMINER	
CHAN, ALEX H	

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2633	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/751,182	Applicant(s) KIM, YONG-SUB	
	Examiner Alex H Chan	Art Unit 2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *5,6,10,11 and 16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-9,12-15 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election in response to Restriction/Election dated October 2, 2003 without traverse of claims 2-4,8,9,12-15 and 21-24 and Group A, including claims 4, 9 and 12-15 in Paper No. 7 is acknowledged. Claims 1 and 7 will also be examined with merits in all groups.

Drawings

2. The drawings are objected to because "opticval output power controller" is cited where "optical output power controller" might have been intended in Fig. 11. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. Figure 1 should be designated by a legend such as "Prior Art" or "Conventional Art" because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claim 1** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,628,214 B1 to Kawase et al (hereinafter Kawase) in view of U.S. Patent No. 6,292,284 B1 to Takauji et al (hereinafter Takauji), and further in view of U.S. Patent No. 4,290,146 to Adolfsson et al (hereinafter Adolfsson).

Regarding claim 1, Kawase in view of Takauji discloses an optical transmission system for compensating for transmission loss, comprising a transmitting apparatus for serializing (20 of Fig. 1, Kawase) a plurality of n-bit channel data (e.g. R, G or B of Fig. 1 and Col. 9, line 58-Col. 10, line 4, Kawase or via data of Fig. 5, Takauji), where n is a natural number, received from an external source (e.g. 10 of Fig. 1, Kawase), in response to a predetermined clock signal (via CL0/CL1 and 30 of Fig. 1, Kawase or clock of Fig. 5, Takauji), converting the serialized channel data and the predetermined clock signal into a current signal (e.g. electric signals via 40-1 of Fig. 1 and Col. 9, lines 26-29, Kawase or Col. 15, lines 19-21, Takauji), the magnitude of which changes in accordance with an error detection signal (e.g. 107 produces an LD driving control signal for automatic light power control according to difference between reference and monitoring voltage, Col. 2, lines 11-21 or via 60 of Fig. 5 and Col. 40, lines 10-16, Takauji), and outputting optical signals having optical output power corresponding to the magnitude of the current signal (Col. 2, lines 54-63 and Col. 40, lines 6-16, Takauji); a first optical fiber (60 of Fig. 1, Kawase or Col. 1, lines 42-49, Takauji) for transmitting the optical signals; a receiving apparatus (108 of Fig. 1, Kawase or 51 of Fig. 5, Takauji) for recovering the n-bit channel data (DA1 of Fig. 1, Kawase) and the predetermined clock signal (output of 160-2 of Fig. 1, Kawase) from the optical signals received through the first optical fiber. However, Kawase in view of

Takauji fails to disclose a receiving apparatus for detecting transmission loss generated when the optical signals are transmitted and received, optically converting the transmission loss, and outputting the optically converted transmission loss as the error detection signal; and a second optical fiber for transmitting the optical converted error detection signal to the transmitting apparatus. Adolfsson discloses a receiving apparatus ("M" of Fig. 1) for detecting transmission loss (e.g. via comparison signal, Col. 11, lines 11-25) generated when the optical signals are transmitted and received, optically converting (via LD2 of Fig. 1) the transmission loss, and outputting the optically converted transmission loss as the error detection signal (e.g. via U_c or feedback and measurement signal, Col. 8, lines 9-15 and Col. 11, lines 26-30); and a second optical fiber (LC3 of Fig. 1) for transmitting the optical converted error detection signal to the transmitting apparatus ("S" of Fig. 1). Accordingly, one of the ordinary skilled in the art would have been motivated to employ the above means for automatically compensating for variations in signal attenuation along the optical link (Col. 2, lines 8-11). Therefore, it would have been obvious to one of artisan skilled in the art to modify the data transmission system of Kawase in view of Takauji by incorporating the above means as taught by Adolfsson because it compensates for variations in signal attenuation along the optical link.

Regarding claim 2, Kawase in view of Takauji and Adolfsson discloses a first phase locked loop (30 of Fig. 1, Kawase) for generating a clock signal (CL1 of Fig. 1, Kawase) synchronized with the predetermined clock signal (CL0 of Fig. 1, Kawase) as a first synchronized clock signal and outputting the first synchronized clock signal as an actual clock

signal for data transmission (Col. 9, lines 1-9, Kawase); a parallel/serial data converter (20 of Fig. 1, Kawase) for receiving a plurality of n-bit channel data (e.g. R, G, B, H-Sync and V-Sync of Fig. 1, Kawase) in response to the first synchronized clock signal, serializing the n-bit channel data in response to the first synchronized clock signal, and outputting the serialized n-bit channel data (Col. 9, line 58-Col. 10, line 4, Kawase), a receiver optical diode (51 of Fig. 5, Takauji or PD3 of Fig. 1, Adolfsson) for receiving and converting the error detection signal transmitted from the second optical fiber (Col. 1, lines 42-49, Takauji or LC3 of Fig. 1, Adolfsson) into a current signal (e.g. an electric signal) and outputting the current signal (Col. 2, lines 4-10, Takauji or Col. 5, lines 53-56, Adolfsson); an error compensating optical driver (e.g. combination of 102, 107, 106, 103 and 105 of Fig. 22 or 30 of Fig. 5, Takauji) for converting (e.g. via 108 of Fig. 22 or 21 of Fig. 5, Takauji) the serialized channel data (e.g. output of 20 of Fig. 1, Kawase or via transmitting data of 21 of Fig. 5, Takauji) and the first synchronized clock signal (e.g. CL1 of Fig. 1, Kawase or via clock of Fig. 5, Takauji) into current signals (Col.1, lines 59-67, Takauji), changing the magnitudes of the converted current signals in accordance with the current signal output by the receiving optical diode (e.g. 107 produces an LD driving control signal for automatic light power control according to difference between reference and monitoring voltage, Col. 2, lines 11-21 or via 60 of Fig. 5 and Col. 40, lines 10-16, Takauji, or via regulator means, Col. 11, lines 21-25, Adolfsson), and outputting the current signals as driving signals (Col. 2, lines 46-53 and Col. 39, lines 62-67, Takauji); and a plurality of transmitting optical diodes (10 of Fig. 5, Takauji or LD4 and LD6 of Fig. 3, Adolfsson) for outputting optical signals having optical output power corresponding to the driving signals (Col. 2, lines 54-63, Takauji).

6. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawase in view of Takauji and Adolfsson as applied to claim 1 above, and further in view of U.S. Patent No. 5,018,142 to Simcoe et al (hereinafter Simcoe).

Regarding claim 3, Kawase in view of Takauji and Adolfsson discloses all limitations as discussed above, but fails to discloses an optical transmitting apparatus comprising a data latch for receiving the n-bit channel data and segmenting and latching the n-bit channel data by N (N is a natural number) bits in response to first through m (m is a natural number) latch clock signals; and a data serializer for performing a logic operation on the n-bit channel data latched by the data latch, first through nth non-overlapping clock signals, and inverted first through nth non-overlapping clock signals and outputting the logic operation result as the serialized channel data, wherein the first through nth non-overlapping clock signals are generated by the phase locked loop (PLL) and have a predetermined offset so as not to overlap each other. Simcoe discloses a transmitting section (1 of Fig. 1) comprises a data latch (108, 112 and 120 of Fig. 4) for receiving the n-bit channel data (2 of Fig, 4) and segmenting and latching the n-bit channel data by N (N is a natural number) (e.g. 16 bits into 16 lines) in response to first through mth (m is a natural number) latch clock signals (e.g. via 20 of Fig. 4 and Col. 35, lines 28-39); and a data serializer (44 of Fig. 3) for performing a logic operation on the n-bit channel data latched by the data latch (via 28, 32, 36 and 40 of Fig. 3), first through nth non-overlapping clock signals (via SYNC1, SYNC2 and BIT CLOCK of Fig. 3) and inverted first through nth non-overlapping clock signals (e.g. via COMPLEMENT and 36 of Fig. 3) and outputting the logic operation result as the serialized channel data (Col. 31, lines 9-46). Accordingly, one of the ordinary skilled in the art would have been motivated to employ a data latch and a serializer for providing

a new and improved system for transmitting digital data, and in particular, for organizing and coding binary data from a plurality of data lines for transmission over a fiber optic link (Col. 2, lines 32-36). Therefore, it would have been obvious to one of artisan skilled in the art at the time the invention was made to modify the data transmission system of Kawase in view of Takauji and Adolfsson by incorporating a data latch and serializer because this provides providing a new and improved system for transmitting digital data over a fiber optic link.

Regarding claim 4, Takauji discloses all limitations as discussed above, and further discloses an optical receiver (51 of Fig. 5) for receiving the error detection signal (e.g. in the form of monitoring light), converting the received error detection signal into a voltage signal, converting the level of the converted voltage signal (e.g. via 50 of Fig. 5), and outputting a digitized error compensation signal (e.g. via 61 of Fig. 5); a transmission loss compensator (e.g. 70 and 62 of Fig. 5) for recovering transmission loss data in each channel from the error compensation signal (via identifying the variance in the outputs of 61 of Fig. 5)in response to the first synchronized clock signal (via clock of 70 of Fig. 5 and Col. 16, lines 48-49 and Col. 15, lines 61-67), analog converting (via 63 of Fig. 5) the recovered transmission loss data, and generating analog converted transmission loss data as transmission loss compensation signals (Col. 18, lines 44-47); an optical output controller (e.g. controller inside 63 of Fig. 5) for generating optical output control signals (e.g. VPCNT of Fig. 5) in response to the transmission loss compensation signals (Col. 18, lines 48-67).

Regarding claim 7, Kawase in view of Takauji and Adolfsson teaches all limitations as claimed in claim 7, but does not explicitly disclose an electrical transmission line for transmitting error detection signal to the transmitting apparatus. However, since Adolfsson suggests that optical link will be much safer than an electrical signal line when used in an environment having combustible or explosive material (Col. 1, lines 33-45), it would have been a matter of design choice to employ an electrical transmission lone for transmitting the error detection signal depending on design requirement and specification. This support rational is based on a recognition that the claimed differences exist not as a result of an attempt by applicant to solve a problem but merely amounts to selection of expedient known to the artisan of ordinary skill as design choice.

Regarding claims 8 and 12, the limitations introduced by claims 8 and 12 correspond to the limitations introduced by claim 2. The treatment of claim 2 above reads on the corresponding limitations of claims 8 and 12.

Regarding claims 9 and 13, the limitations introduced by claims 9 and 13 correspond to the limitations introduced by claim 4. The treatment of claim 4 above reads on the corresponding limitations of claims 9 and 13.

7. **Claims 14-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawase in view of Takauji and Adolfsson as applied to claim 1 above, and further in view of U.S. Patent No. 6,195,370 B1 to Haneda et al (hereinafter Haneda).

Regarding claims 14-15, Kawase in view of Takauji and Adolfsson fails to disclose the optical output controller generates the optical output control signals so as to change the modulation current or the bias current of the driving signals in response to the transmission loss compensating signals. Haneda discloses a optical output controller (111 of Fig. 1, Col. 9, lines 24-48) generates the optical output control signals so as to change the modulation current or the bias current (Col. 16, lines 27-32) of the driving signals in response to the transmission loss compensating signals (e.g. via detecting an abnormal variation in modulation or bias current via 170 of Fig. 1 and Col. 9, lines 49-67). Accordingly, one of the ordinary skilled in the art would have been motivated to generate an optical output control signal so as to change the modulation or bias current of the driving signals in order to reduce failure and emission delay to the minimum with respect to deterioration in characteristic of a laser diode due to a change in ambient temperature and secular changes to thereby make it possible to hold an optical output constant (Col. 2, lines 34-39). Therefore, it would have been obvious to one of artisan skilled in the art to modify the data transmission system of Kawase in view of Takauji and Adolfsson by generating an optical output control signal so as to change the modulation and bias current of the driving signals as suggested by Haneda because this makes it possible to hold an optical output constant.

8. **Claim 21** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawase in view of Takauji and Adolfsson as applied to claim 1 above, and further in view of U.S. Patent No. 6,211,714 B1 to Jeong.

Regarding claim 21, Kawase in view of Takauji and Adolfsson discloses all limitations as discussed in claim 1, but fails to disclose a parallel/serial data converting circuit of a transmitting apparatus, comprising a PLL for generating first through nth non-overlapping clock signals having a predetermined offset so as not to overlap each other and inverted first and nth nonoverlapping clock signals obtained by inverting the first through nth non-overlapping clock signals, the parallel/serial data converting circuit for converting n-bit channel data input from the outside into serial information data in response to the first through nth overlapping clock signals and transmitting the serial information data. Jeong discloses a parallel/serial data converting circuit of a transmitting apparatus (15 of Fig. 1), comprising a PLL (PLL, 60 of Fig. 2 or Fig. 3, Col. 5, lines 66-67) for generating first through nth non-overlapping clock signals (e.g. φ1-φ9 of Fig. 6) having a predetermined offset (Fig. 5 and Col. 7, lines 66-67) so as not to overlap each other (e.g. via clock signal delay, Fig. 5) and inverted first and nth nonoverlapping clock signals obtained by inverting (e.g. via inversion terminal) the first through nth non-overlapping clock signals (Col. 8, lines 48-60), the parallel/serial data converting circuit for converting n-bit channel data input (e.g. DATA[0]-DATA [7] of Fig. 6) from the outside into serial information data (SERIAL DATA of Fig. 6) in response to the first through nth overlapping clock signals and transmitting the serial information data (Col. 3, lines 61-64). Accordingly, one of the ordinary skilled in the art would have been motivated to employ the above means to provide a high speed data serializer capable of converting parallel data to serial data at speeds greater than one GB/s,

and a data/clock recovery circuit that does not require an individual independent clock for each channel (Col. 1, line 65-Col. 2, line 3). Therefore, it would have been obvious to one of artisan skilled in the art to modify the data transmission system of Kawase in view of Takauji and Adolfsson by incorporating a PLL in a parallel/serial data converting circuit of a transmitting apparatus suggested by Jeong because this provides a data/clock recovery circuit that does not require an individual independent clock for each channel.

Regarding claim 22, Jeong discloses that the predetermined offset corresponds to the width of the unit bit of the serial information data (e.g. each cycle of TX_Serial of Fig. 22 corresponds to width of unit bit D0-D19 serial data).

Regarding claim 23, Kawase in view of Takauji, Adolfsson and Jeong does not explicitly disclose the first through nth latch clock signals have timing margins corresponding to N unit bits among the first through nth non-overlapping clock signals and the first latch clock signal is the non-overlapping clock signal having the largest timing margin with respect to the first non-overlapping clock signal. However, it would have been a matter of design choice to utilize a large or largest timing margin with respect to non-overlapping clock signal, depending on the application specification and requirement. This support rational is based on a recognition that the claimed differences exist not as a result of an attempt by applicant to solve a problem but merely amounts to selection of expedient known to the artisan of ordinary skill as design choice.

9. **Claim 24** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawase in view of Takauji, Adolfsson and Jeong above, and further in view of U.S. Patent No. 6,363,441 B1 to Bentz et al (Hereinafter Bentz).

Regarding claim 24, Kawase in view of Takauji, Adolfsson and Jeong does not explicitly disclose a first logic operator realized by n NAND operators corresponding to the bits of the n bit channel data and the first through nth non-overlapping clock signals, and the inverted second through inverted first non-overlapping clock signals, the NAND operators for performing a NAND operation on the respective bits of the n-bit channel data, the non-overlapping clock signals, and the inverted non-overlapping clock signals; a second logic operator realized by p NAND operators for segmenting the output data of the n NAND operators into p groups and performing a NAND operation on the segmented data; and an OR operator for performing an OR operation on the output data of the second logic operator.

Bentz discloses a data serializer (Fig. 10) comprises: a first logic operator realized by n NAND operators (e.g. 1070-1077 of Fig. 10); a second logic operator realized by p NAND operators (1090-1092 of Fig. 10) for segmenting the output data of the n NAND operators into p groups and performing a NAND operation on the segmented data (or via 1400 of Fig. 14 for segmentation); and an OR operator (1093A-1095B of Fig. 10) for performing an OR operation on the output data of the second logic operator. Accordingly, one of the ordinary skilled in the art would have been motivated to employ the above means for providing an architecture that facilitates the utilization of parallel and sequential graphics processing and communication hardware in an effective and efficient manner to support retrieval of information (Col. 3, lines 23-27). Therefore, it would have been obvious to one of artisan skilled in the art to modify the

data transmission system of Kawase in view of Takauji, Adolfsson and Jeong by incorporating the aforementioned NAND and OR gates as taught by Bentz for operating on the respective bits of the n-bit channel data, the non-overlapping clock signals and the inverted non-overlapping clock signals as discussed by Jeong because this provides an architecture that facilitates the utilization of parallel and sequential graphics processing and communication hardware in an effective and efficient manner to support retrieval of information.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Farhan is cited to show a controller, A/D, clock signal in and P/S of an optical transmitter (Fig. 5 and 8). Kikuchi is cited to show a signal transmitter comprising parallel and serial converter having R, G, B and sync as inputs with PLL as clocking signal (Fig. 1). Kosugi et al is cited to illustrate an optical transmitter having a parallel/serial conversion circuit, a receive and reference clock and a bias drive circuit (Fig. 6). Mihara et al is cited to show a wavelength controller, a noise detection circuit and an automatic gain control (Fig. 6B). Oda et al is cited to show a LD driver having automatic power control, VTC, AGC and data and clock signal as input (Fig. 12). Morita et al is cited to show a LD driving circuit control section and light detection section as well as a light output level variation circuit (Fig. 9 and 10). Okada is cited to show another P/S, carrier detection and a timing generator (Fig. 13). Link et al is cited to show an error circuit and an updating circuit for updating bias and modulation current (Fig. 1). Feldman et al is cited to show a clock control, power control, a modulation DAC, power level

monitor and a laser diode (Fig. 3). Knecht is cited to demonstrate an optical transmitter for detecting serial inputs and an encoder for encoding serial data (Fig. 2-4). Ishizuka et al is cited to show a code detection circuit and a control circuit for providing coding signals to laser (Fig. 11).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alex H Chan whose telephone number is (703) 305-0340. The examiner can normally be reached on Monday to Friday (8am to 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (703) 305-4729. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Alex Chan
Patent Examiner, Art Unit 2633
December 5th, 2003

Leslie Pascal
LESLIE PASCAL
PRIMARY EXAMINER